REMARKS

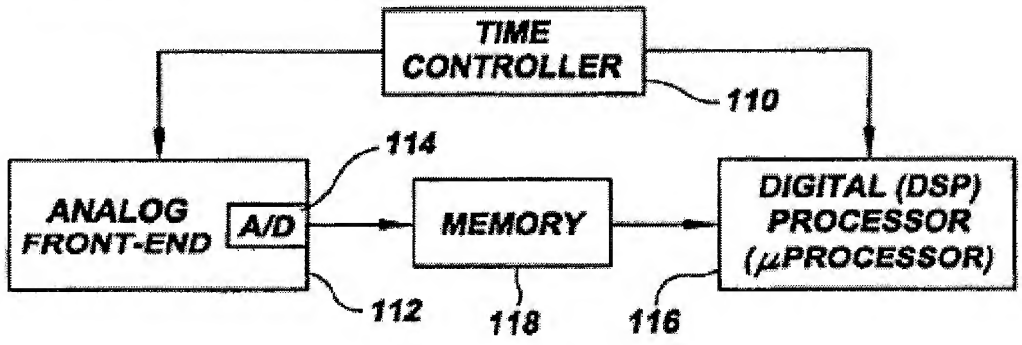
Claims 1-56 are pending in this application. Reconsideration and allowance of the application are respectfully requested.

In the instant Final Office Action dated January 9, 2008, claims 1-56 stand rejected under 35 U.S.C. § 103(a) over Shaeffer *et al.* (U.S. Patent No. 6,963,626) in view of Hadwiger *et al.* (U.S. Patent No.6,738,845).

Each rejection relies upon a similar combination of elements from the two cited references. Applicant notes that while the elements of the cited references are identified, little explanation of how these elements are combined is provided. In an effort to facilitate prosecution, Applicant assumes that the asserted combination attempts to create a hypothetical embodiment as described below. To that end, the following discussion is provided. Should Applicant's interpretation be incorrect, Applicant requests that the Examiner provide clarification and afford Applicant with an opportunity to respond as required, for example, by 35 U.S.C § 132.

The Examiner's combination relies upon elements present in both of the block diagrams shown in FIGs. 1 and 2 of Shaeffer. As discussed in Shaeffer and relied upon in the rejection, the DSP 116 can be powered down when the analog front-end 114 is active (*see, e.g.*, Shaeffer at Col. 5, lines 47-62). FIG. 1 is reproduced below:

FIG. 1
RECEIVER BLOCK DIAGRAM



The Examiner's combination further relies upon elements present in the block diagram of FIG. 2 of the Hadwiger reference. As discussed in Hadwiger and relied upon in the rejection, the bus arbitration module (BAM) 211 arbitrates between the DSP system 201 and various devices (*see, e.g.*, Hadwgier at Col. 4, lines 31-55). FIG. 2 is reproduced below.

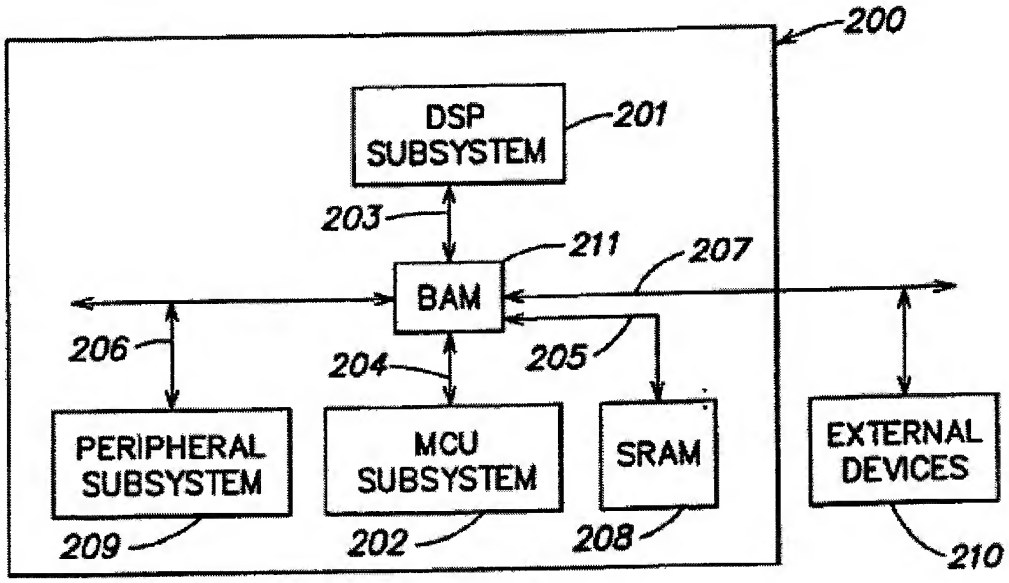


FIG. 2

As best as can be determined, the Examiner's combination proposes adding the BAM and peripherals of FIG. 2 to DSP 116 of FIG. 1 (e.g., DSP 116 essentially replaces DSP subsystem 201). This results in a system similar to the combined FIGs. 1 and 2 shown below.

FIG.1
RECEIVER BLOCK DIAGRAM

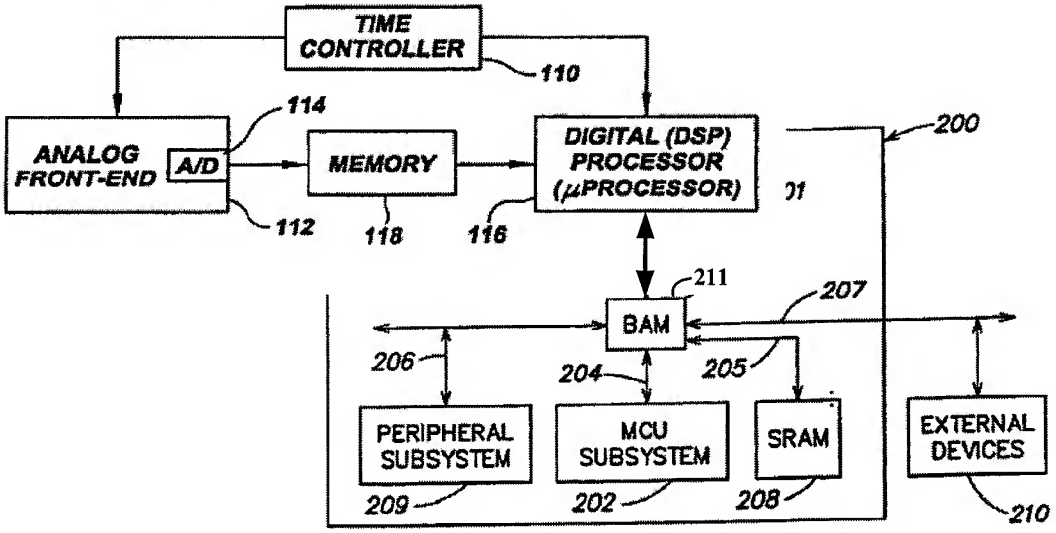


FIG. 2

It should be apparent that

1) when deactivated by time controller 110, DSP 116 would not issue any requests, and

2) arbitration decisions of BAM 211 are not responsive to time controller 110.

Should the Examiner have envisioned some, as of yet unidentified, combination of the references, Applicant requests clarification, a showing of support and an opportunity to respond pursuant to M.P.E.P. § 706.07 ("The examiner should never lose sight of the fact that in every case the applicant is entitled to a full and fair hearing, and that a clear issue between applicant and examiner should be developed, if possible, before appeal."). The following discussion explains why the aforementioned elements are relevant to the lack of correspondence between the asserted combination and the claimed limitations.

With particular regard to claims 1-41 and 49-56, the Examiner's argument in the Final Office Action of January 9, 2008 (hereafter "the Examiner's response"), does not address each claim limitation. Aspects of Applicant's claimed invention allow for a bus master to continue operating while, for example, running a transition interrupt procedure (*see, e.g.*, Applicant's Specification at paragraphs 35-41). In some implementations,

other bus masters continue to operate and therefore may issue access requests; the AHB bus is capable of restricting those access requests. Thus, there is a clear (and often important) differentiation between restricting an "*issued* access request" and shutting down a bus master so that no requests issue. Claims 1-41 and 49-56 each include limitations directed to restricting *issued* access requests. This is in contrast to the Examiner's asserted combination, which would restrict accesses only to the extent that requests are prevented from ever issuing.

Accordingly, Applicant respectfully submits that the Examiner's definition of restriction, which states that in the prior art "no access requests would be generated, and thus, there would be no access requests to restrict," does not address each claim limitation (*see also*, Applicants argument of July 25, 2007 (hereafter "Applicant's previous response" and incorporated herein by reference)). Put another way, various claim limitations are directed to restricting *issued* (past tense) requests. Thus, the claim limitations are directed to restriction of a request that has been issued. These limitations cannot be met by simply preventing an access request from issuing because the limitations require that the access request actually issues. As such, the Examiner's asserted prior art does not correspond because no issued requests are restricted.

With particular regard to claims 42-48, Applicant respectfully submits that the Examiner's response fails to show correspondence to each claim limitation. For example, claim 42 includes limitations directed to the bus arbiter implementing a less favorable arbitration policy. Neither reference alone or in combination teaches or suggests a bus arbiter that implements a less favorable arbitration policy. Instead, the Shaeffer reference merely teaches powering down the processor, while the Hadwiger reference merely teaches a bus arbiter. As the Examiner's response merely identifies elements of the Shaeffer and Hadwiger reference (*i.e.*, a shut down signal and an arbiter), there is no support in the record for a modification to the arbiter of Hadwiger. Instead, as asserted by the Examiner's response, the combination merely includes the power down signal of the Shaeffer reference and the arbiter of the Hadwiger reference. Put another way, Hadwiger appears to teach that the arbiter merely maintains the same arbitration policy and the Shaeffer reference does not teach or suggest modifying an arbiter. Thus, regardless of whether the processor is powered down as taught by Shaeffer, the arbiter

maintains the same arbitration policy. As the arbiter of Hadwiger neither 1) responds to any signal indicating a change to an active mode, nor 2) implements a less favorable arbitration policy, the combination fails to correspond to each claimed limitation.

With respect to the Examiner's response stating that:

> the independent claim language states communication apparatus **comprising** (emphasis added):
> The broad specification would afford elements defined in addition to other elements.

(Examiner's response at page 11, lines 3-8), Applicant respectfully submits that Applicant's specification and claim language is improper basis for supporting the Examiner's prior art combination. The M.P.E.P. is clear that it is improper for the Examiner to use the Applicant's specification to provide a support for the combination of elements as a judgment on obviousness should not include knowledge gleaned only from an applicant's disclosure. See M.P.E.P. § 2145.

Moreover, Applicant maintains (as stated in Applicant's previous response) that it is not possible to be certain, with any particularity, what the Examiner's asserted combination includes and/or how any such combination would function. As discussed in Applicant's previous response, the cited portions do not provide clarification regarding how one of skill in the art would combine the references or how such a combination would function. Without clarification of how the asserted combination would function (and support for such functionality in prior art) the Examiner has done little more than identify elements of the prior art. To establish a *prima facie* case of obviousness the Examiner must provide a reason to combine the elements. Applicant respectfully submits that the specifics of how the asserted elements would function together are necessary to 1) judge whether the combination (not just the individual elements) in fact corresponds to the claimed invention and 2) determine whether a proper reason to combine the elements exists. As the record, including the cited references and the Examiner's response, is deficient regarding support for such details, Applicant submits the rejections are improper and cannot stand.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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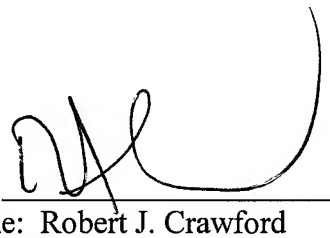
By: 
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